23. (Twice amended) A structure comprising a varactor which comprises:

a plate region and body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode;

a dielectric layer situated over the semiconductor body and contacting the body region; and

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a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage differing from the plate-to-body voltage, the gate-to-body voltage varying as a function of the plate-to-body voltage as the plate-to-body voltage is varied during operation of the varactor to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

29. (Amended) A structure as in Claim 28 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

B3

31. (Amended) A structure as in Claim 30 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

B4

32. (Twice amended) A structure comprising:

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a plate region and a body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions extending to a primary surface of the semiconductor body and meeting each other to form a p-n junction, the plate region comprising a main plate portion and a plurality of finger portions continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body

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SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

region therealong, at least two of the finger portions extending longitudinally non-parallel to one another;

a dielectric layer situated over the semiconductor body and contacting the plate region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region.

B5 Cont.

38. (Twice amended) A method comprising:

selecting a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a dielectric layer situated over the semiconductor body and contacting the body region, (c) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, and (d) a plate electrode and a body electrode respectively connected to the plate and body regions, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region selectively appearing and disappearing in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and body electrodes is varied during operation of the varactor, the inversion layer occupying a lateral inversion area along the primary surface, the varactor having a maximum capacitance dependent on the inversion area in combination with the plate area; and

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adjusting the plate and inversion areas to control the minimum and maximum capacitances of the varactor.

43. (Amended) A method as in Claim 38 wherein the gate electrode is at a gate-to-body bias voltage relative to the body electrode, the method further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

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44. (Amended) A method as in Claim 38 wherein the gate electrode is at gate-to-body bias voltage relative to the body electrode, the method further including causing the gate-to-

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(408) 453-9200
FAX (408) 453-7979

B7 cont.

body voltage to differ from the plate-to-body voltage and to vary as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

B8

50. (Amended) A structure as in Claim 47 wherein the circuitry comprises an inductor.--

Enclosed is an appendix which indicates how the above version of Claims 20, 23, 29, 31, 32, 38, 43, 44, and 50 is produced from the previous version of those claims. In the appendix, added material is underlined, and deleted material is in brackets.

Add new Claims 67 - 88 as follows:

--67. A structure as in Claim 63 wherein the varactor includes a plate electrode and a body electrode respectively connected to the plate and body regions, an inversion layer that meets the plate region selectively appearing and disappearing in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and body electrodes is varied during operation of the varactor.

68. A structure as in Claim 65 wherein at least two of the finger portions extend longitudinally non-parallel to another.

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69. A structure as in Claim 17 wherein an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode as the plate-to-body voltage is varied during operation of the varactor.

70. A structure as in Claim 32 further including a plate electrode and a body electrode respectively connected to the plate and body regions, an inversion layer that meets the plate region selectively appearing and disappearing in the body region below the gate electrode as a plate-to-body bias voltage applied between the plate and the body electrodes is varied during operation of the structure.

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71. A method comprising:

providing a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the

plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

applying (a) a plate-to-body bias voltage between the plate and body electrodes and (b) a gate-to-body bias voltage between the gate and body electrodes; and

varying the plate-to-body voltage while maintaining the gate-to-body voltage approximately constant to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

72. A method as in Claim 71 further including providing componentry for maintaining the gate-to-body voltage approximately constant.

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73. A method as in Claim 71 wherein the plate and body regions extend to a primary surface of the semiconductor body, the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

74. A method as in Claim 71 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

75. A method as in Claim 71 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

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76. A method as in Claim 75 wherein the gate electrode is situated outside the capacitance signal path.

77. A method as in Claim 71 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

78. A method as in Claim 77 wherein the gate electrode is situated outside the inductance-capacitance signal path.

79. A method comprising:

providing a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

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applying (a) a plate-to-body bias voltage between the plate and body electrodes and (b) a gate-to-body bias voltage between the gate and body electrodes; and

varying (a) the plate-to-body voltage and (b) the gate-to-body voltage as a function of the plate-to-body voltage as the plate-to-body voltage is varied to cause an inversion layer that meets the plate region to selectively appear and disappear in the body region below the gate electrode.

80. A method as in Claim 79 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

81. A method as in Claim 79 further including providing componentry for causing the gate-to-body voltage to vary as a function of the plate-to-body voltage.

82. A method as in Claim 79 wherein the componentry causes the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.

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83. A method as in Claim 79 wherein the plate and body regions extend to a primary surface of the semiconductor body, the plate region occupies a lateral plate area along the

primary surface, the varactor has a minimum capacitance dependent on the plate area, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

84. A method as in Claim 79 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

85. A method as in Claim 79 further including providing electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

B9 cont

86. A method as in Claim 85 wherein the gate electrode is situated outside the capacitance signal path.

87. A method as in Claim 79 further including providing electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

88. A method as in Claim 87 wherein the gate electrode is situated outside the inductance-capacitance signal path.--

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(408) 453-9200
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